LISTING OF CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor integrated circuit device including a clock synchronous type circuit that operates in synchronization with one of a rising edge ~~flank~~ and a falling edge ~~flank~~ of a reference clock and a plurality of clock buffer circuits for distributing a reference clock to said clock synchronous circuit, wherein each of said clock buffer circuits comprises ~~a second-stage~~ an inverter including:

a first~~, P-type,~~ transistor of a first conductivity type for driving a load at one ~~of edges flank~~ edge of the reference clock ~~with which~~ when said clock synchronous circuit does not operate in synchronization; and

a second~~, N-type,~~ transistor of a second conductivity type for driving the load at the other edge ~~flank~~ of the reference clock ~~with which~~ when said clock synchronous circuit operates in synchronization, the second transistor having a current supply ability ~~being formed to have a gate width equal or~~ larger than ~~a gate width of~~ the first transistor.

2. (Original) The semiconductor integrated circuit device according to claim 1, wherein the first transistor is a P-channel field-effect transistor; the second transistor is an N-channel field-effect transistor; and said clock synchronous circuit operates in synchronization with the falling edge flank of the reference clock.

3. (Currently Amended) The semiconductor integrated circuit device according to claim 1, wherein said first transistor has a gate width set to a gate width value that produces a change in the edge flank that is slowed down, and the gate width value being selected so that a pulse waveform of the reference clock is not destroyed.

4. (Original) The semiconductor integrated circuit device according to claim 1, comprising: a first-stage inverter displaced in an input stage of said each of said clock buffer circuits, the first-stage inverter comprising:

an N-channel field-effect transistor having a gate width set properly based on an input capacity of the inverter; and

an P-channel field-effect transistor having a gate width larger than the N-channel field-effect transistor.

5. (Original) The semiconductor integrated circuit device according to claim 2, comprising: a first-stage inverter displaced in an input stage of said each of said clock buffer circuits, the first-stage inverter comprising:

an N-channel field-effect transistor having a gate width set properly based on an input capacity of the inverter; and

an P-channel field-effect transistor having a gate width larger than the N-channel field-effect transistor.

6. (Original) The semiconductor integrated circuit device according to claim 1, comprising: a gate circuit displaced in an input stage of said each of said clock buffer circuits, for supplying the reference clock to the inverter according to an enable signal, the gate circuit comprising:

an N-channel field-effect transistor having the gate width set properly based on an input capacity of the inverter; and

an P-channel field-effect transistor having the gate width larger than the N-channel field-effect transistor.

7. (Original) The semiconductor integrated circuit device according to claim 2, comprising: a gate circuit displaced in an input stage of said each of said clock buffer circuits, for supplying the reference clock to the inverter according to an enable signal, the gate circuit comprising:

an N-channel field-effect transistor having the gate width set properly based on an input capacity of the inverter; and

an P-channel field-effect transistor having the gate width larger than the N-channel field-effect transistor.

8. (Original) The semiconductor integrated circuit device according to claim 6, wherein the gate circuit is a NAND gate.

9. (Original) The semiconductor integrated circuit device according to claim 1, having a clock tree synthesis configuration made up using said clock buffer circuits.

10. (New) The semiconductor integrated circuit device according to claim 1, wherein said first transistor is connected between a first voltage supply line and an output terminal to be connected to said clock synchronous circuit, and said second transistor is connected between a second voltage supply line and an output terminal.

11. (New) A semiconductor integrated circuit device including a clock buffer, said clock buffer comprising:

a first transistor having a first conductivity type and a first current supply ability, said first transistor being connected between a first voltage supply line and an output terminal to be connected to a clock synchronous type circuit, said clock synchronous type circuit operating in synchronization with one of either a rising edge and a falling edge; and

a second transistor having a second conductivity type and a second current supply ability, said second transistor being connected between a second voltage supply line and said output terminal, said second current supply ability being smaller than said first current supply ability.

12. (New) The device according to claim 11, wherein said first transistor is an N-channel transistor and said second transistor is a P-channel transistor.

13. (New) The device according to claim 11, wherein said first transistor has a gate width larger than a gate width of said second transistor.